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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/434,736	11/02/99	KIM S	000939-07360

020359
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111-3834

MMC2/1109

EXAMINER	
PERT, E	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 11/09/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/434,736	KIM ET AL.	
	Examiner	Art Unit	
	Evan T. Pert	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *08 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-88* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 12, 17, 32, and 41 are objected to because the record is clear that the first contact hole is of substantially equal depth to all the other holes in the first layer, but claims 12, 17, 32, and 41 do not make this clear. Support of the examiner's position is found on page 27 of applicant's response filed 9-8-00, comprising the paragraph starting with "Second.".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gutierrez in view of Hashimoto et al..

Both Gutierrez and Hashimoto et al. teach methods in forming multilevel interconnects. The examiner takes Official Notice that it was well known at the time of applicant's invention that a first set of nodes in a multi-level interconnect could include a junction layer, oxide layer, a gate electrode, and other patterned conductive layers. It was also well known that a second level could include patterned conductive layers isolated by being spaced apart.

Gutierrez teaches a junction layer (116), oxide layer (122), gate electrode (118), patterned conductive layers on the oxide (114), and patterned conductive layers on the first insulating layer (220). The fact that Gutierrez does not teach "exposing the gate electrode" when opening holes in the first layer does not mean "opening a hole over the gate electrode" constitutes an inventive step. It was well known to those of ordinary skill in the art that a gate electrode would need to connect through a layer, and an opening "over the gate electrode" would thus be needed before filling the via.

Gutierrez recognizes that any nodes can be interconnected with his method. Gutierrez teaches that the first and second insulating layers are of essentially uniform thickness. This causes holes in the first layer "to be of substantially equal depth" and holes in the second layer "to be of substantially equal depth." Thus Gutierrez teaches a "two-step" deposition of conductive material, like applicant, where the "second step" forms, for example, plug 220. Guterriez names his resultant conformal layers "conductor-insulator layers" [abstract].

While Gutierrez requires "a seed" for selective deposition, he also teaches that the substrate can act as a seed such that no seeding step is required [col. 5, lines 11-24]. In fact Gutierrez recognizes Tungsten on silicon as useful for selective deposition by CVD [col. 2, lines 63-66 and col. 5, lines 46-52].

Applicant does not teach what methods applicant employs to "not require a seed", but simply relies on the presence of the phrase "selective tungsten thin films 9 by the CVD method" in the specification to enable CVD with "no seeding". Gutierrez

actually explains the entire deposition step that does not require a seed, involving selectively depositing tungsten in a hole with a silicon bottom.

Gutierrez does not teach the advantage of flaring the upper part of the openings in an insulating layer, but Hashimoto et al. do teach creating this shape in a plurality of contact holes in an insulating layer (Ref 44 in Fig. 8A).

It would have been obvious at the time of the claimed invention to have combined the teachings of Gutierrez with Hashimoto et al. to arrive at the claimed invention. One of ordinary skill in the art would have been motivated to use tapered openings to get better step coverage with tighter packing at the bottom of the opening.

Regarding the unique limitation of "by one single step" in claim 5, this has been interpreted simply as meaning that a seeding material need not be deposited, which is clearly anticipated by Guterriez.

Regarding the unique limitation of "in a continuous step" in claim 10, Gutierrez teaches a "continuous step" wherein the gas flow is changed during the step.

Regarding the limitation that the 1st conductive layer is grown over and "extends slightly beyond" the contact holes in the first insulating layer, Hashimoto et al. teach that CVD tungsten could be grown above the holes, and then etched back leaving a landing pad for the next conductive deposit [col. 6, lines 42-45].

Regarding limitation numbers 43 to 57 of the matrix as applied to dependent claims 18, 22, 24, 25, 33, 35, 37, 38, 42, 44-46, 48-54, 58-62, 69-71, 73-79, 83-87, the examiner takes Official Notice that these limitations set forth nothing novel. These limitations were well known teachings within the knowledge of one of ordinary skill in the

art who would have been readily appraised of such upon gaining the teachings of Gutierrez and Hashimoto et al..

Response to Amendment

3. The examiner has presented a matrix of claim limitations in the last Office Action (Paper No. 6). This matrix is presented again, in updated form, based on applicant's amendment.

"X" indicates each newly added limitation. Brackets indicate deletions. For example, "71" is now in brackets since this claim was cancelled.

Furthermore, X* as applied to limitation number 19, indicates that --x-- should have been marked in the first Office Action, but was omitted due to typographical error.

4. The examiner acknowledges applicant's intent to re-submit a formal establishment of ownership [bottom of page 23 of response filed 9-8-00]. However, as of this writing, the re-submitted paper was not matched to the file.

Response to Arguments

5. Applicant's arguments with respect to claims 5-88 have been considered but are moot in view of the new ground(s) of rejection.

6. In view of the newly discovered Hashimoto et al. reference, all previously indicated allowable subject matter is rescinded.

7. Objection to claim 3 withdrawn in view of amendment.

8. In view of applicant's arguments presented on pages 24-25 of the response filed 9-8-00, 112 paragraph 1 rejections are withdrawn.

9. In view of applicant's arguments presented on pages 25-26 of the response filed 9-8-00, 112 paragraph 2 rejections are withdrawn.

10. In view of applicant's arguments presented on page 27 of the response filed 9-8-00, rejections based on recapture are withdrawn, noting that claim objections under item 1 of this Office Action must be addressed.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takahumi et al. are cited for teaching a stepped via wherein "the upper portion is wider than the lower portion".

Flanner is cited for teaching a method of filling via of differing depths with selective CVD.

Flatley et al. is cited for teaching motivation to flare the upper part of a via opening [col. 1, lines 10-23].

MacRae et al. is cited for teaching motivation to flare the upper part of a via opening [col. 1, lines 15-18].

The entire Chapter 4 of Wolf is cited for an overview of the state of the art in multilevel-interconnect technology, well before applicant's claimed invention. Issues such as planarization and selective via filling are discussed at length.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers can be reached on 703-308-2417. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ETP
November 6, 2000

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800

Serial Number 09/434,736
Art Unit 2813

APPENDIX TO OFFICE ACTION (Paper No. 10)

MATRIX OF LIMITATIONS vs. CLAIMS

	CLAIM LIMITATIONS	Independent Claim Number 1	5	6	10	12	15	17	20	23	27	30	31	32	34	36	39	41	66
A	1. Preamble: Method to fill contact holes with metal by 2-step metal deposition process	x	x																
A	2. Preamble: Method of forming a substrate with contact holes			x	x														
A	3. Preamble: Method of forming a **substrate** with contact holes filled by multi-step deposition of conductive layers					x													
A	4. Preamble: Method of forming a **semi-conductor** with contact holes filled by multi-step deposition of **conductive** layers						x	x	x	x	x							x	
A	5. Preamble: Method of forming a **semi-conductor** with contact holes filled by multi-step deposition of **metal** layers											x	x	x	x	x	x		
A	6. provide substrate	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
A	7. substrate is silicon	x	x				X												
A	8. form oxide (e.g. field oxide)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
A	9. form junction layer or "1st and 2nd regions"	x	x	x	x	x			x	x	x	x			x	x	x	X	72
A+D	10. form gate electrode	x	x	x	x		x				x		x				x		
A	11. form "1st conductive pattern"							x	x					x	x			x	x

APPENDIX TO OFFICE ACTION (Paper No. 10)

MATRIX OF LIMITATIONS vs. CLAIMS continued 2 of 5

CLAIM LIMITATIONS	Independent Claim Number																	
form 1st insulating layer on exposed portions of:	1	5	6	10	12	15	17	20	23	27	30	31	32	34	36	39	41	66*
12. the oxide layer	x	x	x	x	x	x		x	x	x	x	x	x	x	x	x	x	x
13. the junction layer	x	x	x	x	x			x		x	x			x	x	x		
14. the gate electrode (or "conductive pattern")	x	x	x	x		x	x	x		x		x	x	x		x	x	x
15. form 1st plurality of contact holes	x	x	x	x	13	x		x	x	x	x	x	x	x	x	x		x
16. form 1st contact hole to expose junction layer and/or 1st conductive pattern					x		x	x			x		x				x	
1st plurality of contact holes or "the hole" exposes: 17. junction layer(s) (or "1st and/or 2nd regions)	x	x	x	x					x	x				x	x	x		80
18. gate electrode(s) or conductive pattern	x	x	x	x		x				x		x		x	x	x	x	x
19. 1st contact holes of substantially equal depth	x	x	x	x	X	x	X	X*	X*	x	x	X*	X	x	x	x	X	x
20. 1st contact holes have tapered upper portion	x	x	x	x	x	x	x	x	x	[29]	x	x	x	x	x	X [40]	56	X [81]
21. fill 1st contact holes with 1st material layer	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
22. form (1st or 2nd) "conductive material" layer into the holes, "entirely"	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
23. first layer is "metal" and is filled into the holes, "entirely"	x	x									x	x	x	x	x	x		

APPENDIX TO OFFICE ACTION (Paper No. 10)

MATRIX OF LIMITATIONS vs. CLAIMS continued 3 of 5

Independent Claim Number

CLAIM LIMITATIONS	1	5	6	10	12	15	17	20	23	27	30	31	32	34	36	39	41	66*
24. fill 1st layer "by one single step"		x																
25. fill 1st layer in holes "in a continuous step"				x														
26. 1st layer is grown over and "extends slightly beyond" first plurality of contact holes	x	x	x	x														
27. form a conductive pattern on 1st insulating layer spaced from 1st metal layer (and/or spaced from 1st conductive material layer)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
28. form a "second conductive pattern"														x			x	x
form 2nd insulating layer on exposed portions of the:																		
29. the conductive layer pattern on 1st insulating layer	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
30. the first insulating layer	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
31. the 1st plurality of holes or single hole	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
32. form 2nd plurality of holes in second insulating layer or single hole	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
33. 2nd plurality of holes are of substantially equal depth	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

APPENDIX TO OFFICE ACTION (Paper No. 10)

MATRIX OF LIMITATIONS vs. CLAIMS continued 4 of 5

CLAIM LIMITATIONS	Independent Claim Number																	
	1	5	6	10	12	15	17	20	23	27	30	31	32	34	36	39	41	66*
2nd plurality of holes formed by removing portions of 2nd insulating layer to expose:																		
34. the first metal layer	x	x									x	x	x	x	x	x		
35. the (2nd) conductive layer pattern	x	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x	
36. the (1st) conductive material layer			x	x	x	x	x	x	x	x							x	
fill (or "form into") a 2nd conductive material layer into 2nd plurality of holes to contact:																		
37. the 1st conductive material layer	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
38. the conductive pattern layer	x	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x	x
39. 1st and/or 2nd layer is metal	x	x			**14**	**16**	**19**	**21**	**26**	**28**	x	x	x	x	x	x		**67**
40. 1st and/or 2nd layers by CVD	**2**		**7**														**57,63**	**82,88**
41. 2nd metal layer "filled in each of the 2nd plurality of contact holes has substantially equal depth"	**3**		**8**															
42. 1st and 2nd metal layers are tungsten	**4**		**9**														**43**	**68**
43. 1st conductive pattern includes gate							**18**	**22**				**33**		**35**			**45**	**69**
44. "1st region" is a junction layer									**24**						**37**			
45. "2nd region" is a gate electrode									**25**						**38**			

APPENDIX TO OFFICE ACTION (Paper No. 10)

MATRIX OF LIMITATIONS vs. CLAIMS continued 5 of 5

CLAIM LIMITATIONS	Independent Claim Number																	
	1	5	6	10	12	15	17	20	23	27	30	31	32	34	36	39	41	66*
46. 1st conductive material layer includes metal A+C																	42	
47. conductive material layer is polysilicon A+C																	44	[71]
48. 1st conductive pattern layer is a gate stack A+C+D																	46	70
49. 1st insulating layer includes oxide A+B																	51	76
50. 2nd insulating layer includes oxide A+B																	59	84
51. forming holes includes use of photoresist A+C																	52,60	77,85
52. forming hole(s) includes wet etch Enable/																	53,61	78, 86
53. forming hole(s) includes dry etch																	54,62	79, 87
54. junction layer includes "P+" doping C																	49	74
55. junction layer includes "N+" doping																	48	73
56. 1st conductive pattern layer includes polysilicon C																	50	75
57. 2nd conductive pattern layer includes polysilicon C																	58	83
58. 1st contact holes have an upper and lower portion width, the lower narrower than the upper										X							X	

A+B+C

G teaching reference